Lab5 Report

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**Introduction**

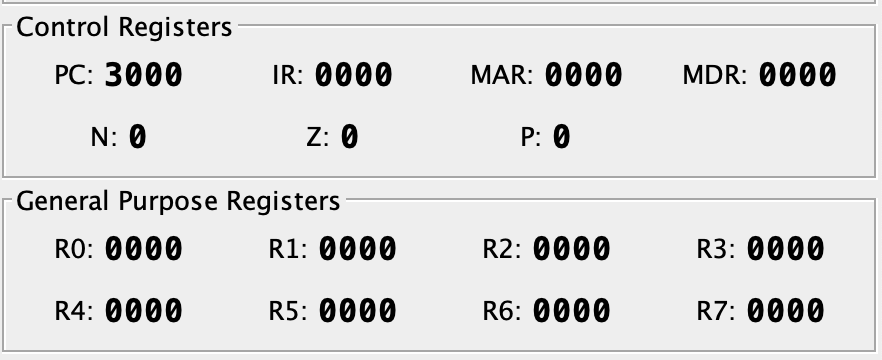
The fetch-decode-execute cycle, also known as the instruction cycle, is the fundamental operational process of a computer's central processing unit (CPU). During each cycle, the CPU retrieves an instruction from memory (fetch), interprets what needs to be done (decode), and performs the necessary actions to complete the instruction (execute). In this report, we analyze the fetch-decode-execute cycle for a sample ADD instruction using a simplified instruction set architecture (ISA) model.

**Chosen Instruction and Initial States**

Instruction: ADD R6, R2, R6

This instruction adds the values in registers R2 and R6 and stores the result in register R6.

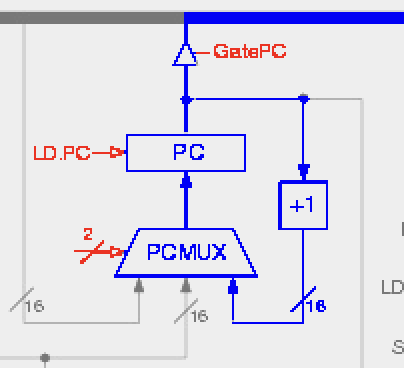
Initial Register and Memory States:



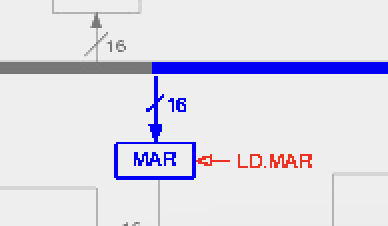
**Detailed Cycle Analysis**

**Fetch Phase**

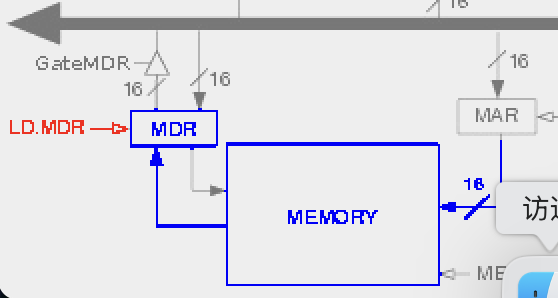
PC becomes PC + 1

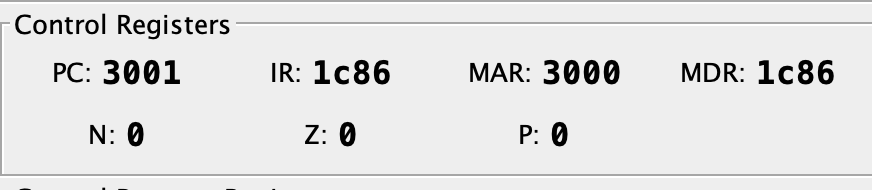


Load contents of PC into MAR, MAR become 3000

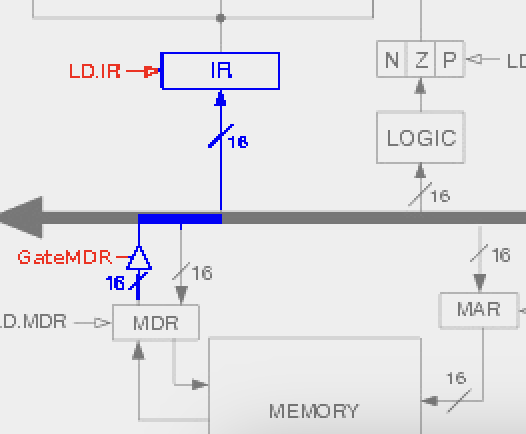
Send a "read" signal from MAR to memory to fetch the instruction, MDR become 1c86

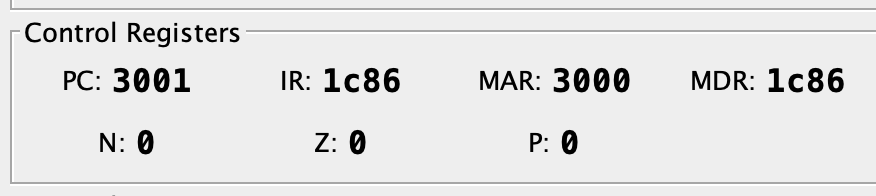




Store the fetched instruction into the Instruction Register (IR).

IR become 1c86 (ADD R6, R2, R6).

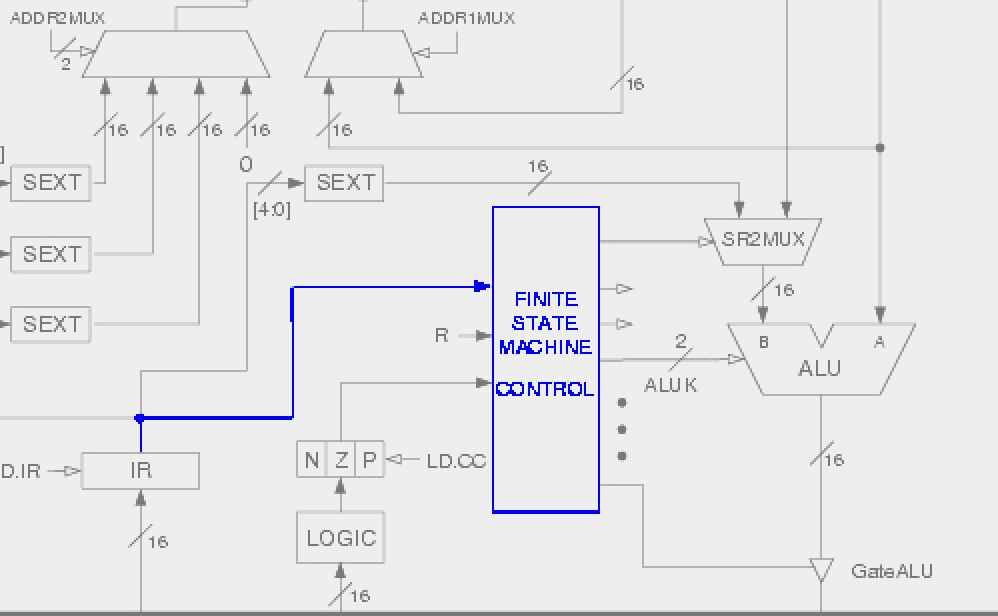




**Decode Phase**

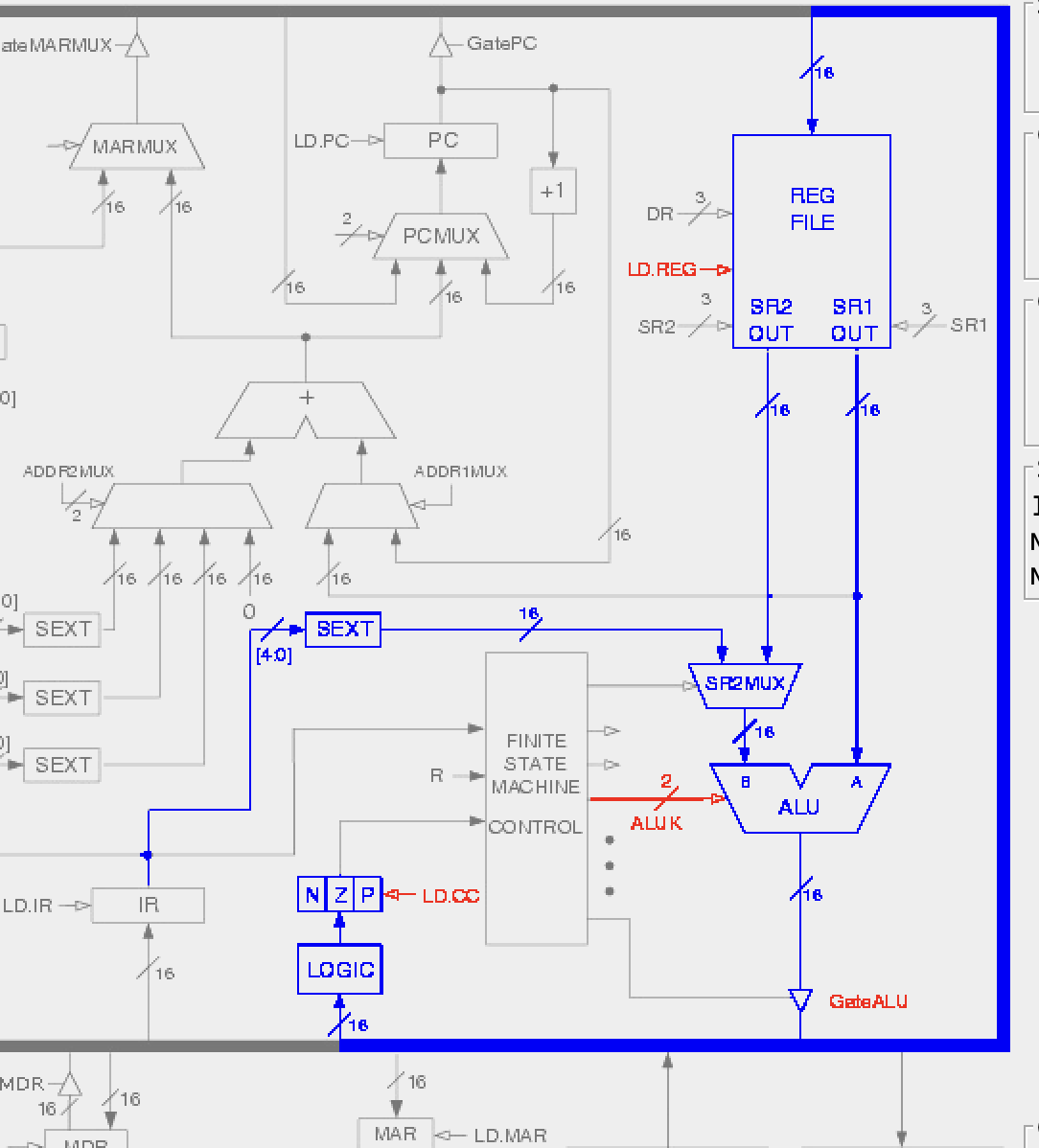
The control unit decodes the instruction in the IR (ADD R6, R2, R6), identifying it as an addition operation involving registers R2 and R6, with the result to be stored in R6.

Control signals are configured to access the ALU for an addition operation and to route the outputs to R1.



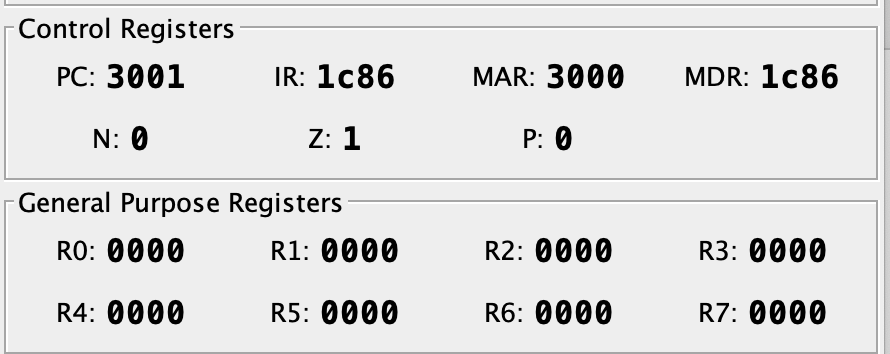
**Execute Phase**

The ALU retrieves the values from registers R2 and R6, performs the addition (0 + 0), and produces the result (0), and set Z = 1.

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**Result**

The result from the ALU (0) is stored in the destination register R6 (0). And Z is set to 1.

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